# BORDERLESS CONTACTS FOR SEMICONDUCTOR DEVICES

## TECHNICAL FIELD

**[0001]** The exemplary embodiments of this invention relate generally to semiconductor structures and, more specifically, relate to borderless contacts for semiconductor devices and the formation thereof.

## BACKGROUND

**[0002]** The following abbreviations are utilized herein:
CA contact area
CD critical dimension
CMOS complementary metal-oxide semiconductor
CVD chemical vapor deposition
DRAM dynamic random access memory
FET field effect transistor
FUSI fully silicided
LPCVD low-pressure CVD
MOSFET metal oxide semiconductor field effect transistor
**[0003]** PECVD plasma-enhanced CVD
**[0004]** RIE reactive ion etch
**[0005]** STI shallow trench isolation
**[0006]** Semiconductors and integrated circuit chips have become ubiquitous within many products due to their continually decreasing cost and size. In the microelectronics industry as well as in other industries involving construction of microscopic structures (e.g., micromachines, magnetoresistive heads, etc.) there is a continued desire to reduce the size of structural features and microelectronic devices and/or to provide a greater amount of circuitry for a given chip size. Miniaturization in general allows for increased performance (more processing per clock cycle and less heat generated) at lower power levels and lower cost. Present technology is at or approaching atomic level scaling of certain micro-devices such as logic gates, FETs and capacitors, for example. Circuit chips with hundreds of millions of such devices are not uncommon. Further size reductions appear to be approaching the physical limit of trace lines and micro-devices that are embedded upon and within their semiconductor substrates. The present invention is directed to such micro-sized devices.
**[0007]** Basically, a FET is a transistor having a source, a gate, and a drain. The action of the FET depends on the flow of majority carriers along a channel between the source and drain that runs past the gate. Current through the channel, which is between the source and drain, is controlled by the transverse electric field under the gate. More than one gate (multi-gate) can be used to more effectively control the channel. The length of the gate determines how fast the FET switches, and can be about the same as the length of the channel (i.e., the distance between the source and drain). Multi-gate FETs are considered to be promising candidates to scale CMOS FET technology down to the sub-22 nm regime.
**[0008]** The size of FETs has been successfully reduced through the use of one or more fin-shaped channels. A FET employing such a channel structure may be referred to as a FinFET. Previously, CMOS devices were substantially planar along the surface of the semiconductor substrate, the exception being the FET gate that was disposed over the top of the channel. Fins break from this paradigm by using a vertical channel structure in order to maximize the surface area of the channel that is exposed to the gate. The gate controls the channel more strongly because it extends over more than one side (surface) of the channel. For example, the gate can enclose three surfaces of the three-dimensional channel, rather than being disposed only across the top surface of the traditional planar channel.
**[0009]** As the CDs of CMOS devices are being aggressively scaled, forming contacts on those small devices is becoming more and more difficult do to the tight overlay tolerance. Borderless contacts and techniques relating thereto help reduce the amount of space required for contacts, and enable production of smaller devices having a tighter pitch. Reference in regard to borderless contacts may be made to: commonly-assigned U.S. Pat. No. 4,944,682 to Cronin et al., commonly-assigned U.S. Pat. No. 4,966,870 to Barber et al. and commonly-assigned U.S. Pat. No. 5,759,867 to Armacost et al.
**[0010]** Borderless contacts have been used in devices with tight pitch, particularly in memory products (e.g., DRAM). Reference in this regard is made to commonly assigned U.S. Pat. No. 6,709,926 to Chidambarrao et al. Borderless contacts are usually formed with a gate stack including a gate dielectric, a gate conductor and an insulating cap. The gate conductor usually comprises polycrystalline silicon (also referred to herein as "poly" or "polysilicon"). In some cases, metal or metal silicide is added on top of the poly in order to lower gate resistance. Reference in this regard may be made to U.S. Pat. No. 5,966,597 to Wright and U.S. Pat. No. 6,236,094 to Wright.
**[0011]** High-k/metal or FUSI gates have been proposed and projected to fulfill future CMOS scaling. A MOSFET with a metal gate can be formed by either so-called "gate-first" techniques or "gate-last" techniques. In a gate-first technique, metal gates are deposited and patterned during gate formation. A poly cap layer on top of the metal layer is usually provided to achieve proper and stable workfunction of the gate stack. It is often further desired to form a silicide on top of the poly cap layer after source/drain formation in order to lower gate resistance. In a gate-last technique, a dummy gate is first formed in order to facilitate transistor formation. The dummy gate is replaced, usually by a high-k/metal gate, after source/drain formation. In a FUSI technique, a poly gate is first formed in order to facilitate transistor formation. The entire portion of the poly gate is then converted to silicide (e.g., after source/drain formation).

## BRIEF SUMMARY

**[0012]** In one exemplary embodiment of the invention, a semiconductor device comprising: a substrate; a borderless contact comprised of a metal; a gate structure on the substrate; a first spacer disposed between the gate structure and the borderless contact and comprised of a first spacer material; an interlevel dielectric that at least partially overlies the gate structure; and a second spacer disposed between at least a portion of the gate structure and the interlevel dielectric and comprised of a second spacer material that is different from the first spacer material.
**[0013]** In another exemplary embodiment of the invention, a method (e.g., to fabricate a semiconductor device having a borderless contact) comprising: forming a first gate structure on a substrate; depositing an interlevel dielectric over the first gate structure; planarizing the interlevel dielectric to expose a top surface of the first gate structure; removing at least a portion of the first gate structure; forming a second gate structure in place of the first gate structure; forming a contact area for the borderless contact by removing a portion of the